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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/998,047 | 11/29/2001 | George John Dawkins | AUS920010973US1 | 6045 |

35525 7590 06/29/2004

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| EXAMINER | |
|---|---|
| BONURA, TIMOTHY M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2114 | |

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/998,047 | DAWKINS ET AL. | |
| | Examiner | Art Unit | |
| | Tim Bonura | 2114 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Arndt, U.S. Patent Number 6,654,906.

3. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

4. Regarding claim 1:

   a. Regarding the limitation of "receiving a system reset interrupt for a logical partition," Arndt discloses a system with the ability to receive indication of an error. (Lines 15-17 of Column 9, see also Figure 6 step 610).

   b. Regarding the limitation of "determining if an operation on the logical partition is being performed at the time the system reset interrupt is received" Arndt discloses a system with the ability to point instructions from one processor to a second processor if

operation are being preformed when an error is received. (Lines 20-25 of Column 9, see also Figure 6 step 612-614).

c. Regarding the limitation of "deferring handling of the system reset interrupt after the operation on the logical partition completed" Arndt discloses a system with the ability to differ the machine code to refresh the primary process until operations are completed. (Lines 20-25 and 28-32 of Column 9, see also Figure 6 step 614-616).

5. Regarding claim 2, Arndt discloses a system with a series of checks which if not passed indicate a rejected request. (Lines 26-34 of Column 7).

6. Regarding claim 3, Arndt discloses a system wherein an error can be a hard error. (Lines 45-53 of Column 8). Arndt also discloses that the error can be a reset error. (Lines 10-14 of Column 8)

7. Regarding claim 4, Arndt discloses a system with checks which set the system into an operating state, or and error state. Arndt also discloses that logic partitions are assigned by the hypervisor. (Lines 1-9 of Column 6). When the hypervisor detects an error condition, a second logic partition is used for backup, the primary logic partition is refreshed and then added back into the logic partition. (Lines 26-34 of Column 8).

8. Regarding claim 5, Arndt disclose a system with a hypervisor that can read a value set by a check of the system. (Lines 26-34 of Column 7). If the checks are not passed a state is state in which the hypervisor does not perform requested functions and error recovery takes place. (Lines 26-34 of Column 7 and Lines 45-53 of Column 8).

9. Regarding claim 6, Arndt discloses a system wherein the hypervisor, upon detecting an error, refreshes the primary copy of the system while continuing to use the secondary copy. (Liens 14-31 of Column 9).

10. Regarding claim 7, Arndt discloses a system that has a checking operation and set condition states. If the checks are not passed a state is state in which the hypervisor does not perform requested functions and error recovery takes place. (Lines 26-34 of Column 7 and Lines 45-53 of Column 8).

11. Regarding claim 8:

d. Regarding the limitation of "receiving a system reset interrupt for a logical partition," Arndt discloses a system with the ability to receive indication of an error. (Lines 15-17 of Column 9, see also Figure 6 step 610).

e. Regarding the limitation of "determining if an operation on the logical partition is being performed at the time the system reset interrupt is received" Arndt discloses a system with the ability to point instructions from one processor to a second processor if operation are being preformed when an error is received. (Lines 20-25 of Column 9, see also Figure 6 step 612-614).

f. Regarding the limitation of "deferring handling of the system reset interrupt after the operation on the logical partition completed" Arndt discloses a system with the ability to differ the machine code to refresh the primary process until operations are completed. (Lines 20-25 and 28-32 of Column 9, see also Figure 6 step 614-616).

12. Regarding claim 9, Arndt discloses a system with a series of checks which if not passed indicate a rejected request. (Lines 26-34 of Column 7).

13. Regarding claim 10, Arndt discloses a system wherein an error can be a hard error. (Lines 45-53 of Column 8). Arndt also discloses that the error can be a reset error. (Lines 10-14 of Column 8)

14. Regarding claim 11, Arndt discloses a system with checks which set the system into an operating state, or and error state. Arndt also discloses that logic partitions are assigned by the hypervisor. (Lines 1-9 of Column 6). When the hypervisor detects an error condition, a second logic partition is used for backup, the primary logic partition is refreshed and then added back into the logic partition. (Lines 26-34 of Column 8).

15. Regarding claim 12, Arndt disclose a system with a hypervisor that can read a value set by a check of the system. (Lines 26-34 of Column 7). If the checks are not passed a state is state in which the hypervisor does not perform requested functions and error recovery takes place. (Lines 26-34 of Column 7 and Lines 45-53 of Column 8).

16. Regarding claim 13, Arndt discloses a system wherein the hypervisor, upon detecting an error, refreshes the primary copy of the system while continuing to use the secondary copy. (Liens 14-31 of Column 9).

17. Regarding claim 14, Arndt discloses a system that has a checking operation and set condition states. If the checks are not passed a state is state in which the hypervisor does not perform requested functions and error recovery takes place. (Lines 26-34 of Column 7 and Lines 45-53 of Column 8). Regarding claim 15:

g. Regarding the limitation of "receiving a system reset interrupt for a logical partition," Arndt discloses a system with the ability to receive indication of an error. (Lines 15-17 of Column 9, see also Figure 6 step 610).

h. Regarding the limitation of "determining if an operation on the logical partition is being performed at the time the system reset interrupt is received" Arndt discloses a system with the ability to point instructions from one processor to a second processor if operation are being preformed when an error is received. (Lines 20-25 of Column 9, see also Figure 6 step 612-614).

i. Regarding the limitation of "deferring handling of the system reset interrupt after the operation on the logical partition completed" Arndt discloses a system with the ability to differ the machine code to refresh the primary process until operations are completed. (Lines 20-25 and 28-32 of Column 9, see also Figure 6 step 614-616).

18. Regarding claim 16, Arndt discloses a system with a series of checks which if not passed indicate a rejected request. (Lines 26-34 of Column 7).

19. Regarding claim 17, Arndt discloses a system wherein an error can be a hard error. (Lines 45-53 of Column 8). Arndt also discloses that the error can be a reset error. (Lines 10-14 of Column 8)

20. Regarding claim 18, Arndt discloses a system with checks which set the system into an operating state, or and error state. Arndt also discloses that logic partitions are assigned by the hypervisor. (Lines 1-9 of Column 6). When the hypervisor detects an error condition, a second logic partition is used for backup, the primary logic partition is refreshed and then added back into the logic partition. (Lines 26-34 of Column 8).

21. Regarding claim 19, Arndt disclose a system with a hypervisor that can read a value set by a check of the system. (Lines 26-34 of Column 7). If the checks are not passed a state is state

in which the hypervisor does not perform requested functions and error recovery takes place. (Lines 26-34 of Column 7 and Lines 45-53 of Column 8).

22. Regarding claim 20, Arndt discloses a system wherein the hypervisor, upon detecting an error, refreshes the primary copy of the system while continuing to use the secondary copy. (Liens 14-31 of Column 9).

23. Regarding claim 21, Arndt discloses a system that has a checking operation and set condition states. If the checks are not passed a state is state in which the hypervisor does not perform requested functions and error recovery takes place. (Lines 26-34 of Column 7 and Lines 45-53 of Column 8).

***Conclusion***

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 7:30-5:00, every other Friday off**. The examiner can be reached at: **703-305-7762**.

25. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Rob Beausoliel.**

- The supervisor can be reached on **703-305-9713.**

26. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

28. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **703-305-3900.**

**29.** Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  **P.O. Box 1450**

  **Alexandria, VA 22313-1450**

Tim Bonura
Examiner
Art Unit 2114

NADEEM IQBAL
PRIMARY EXAMINER

tmb
June 24, 2004